Digital Design Using Digilent FPGA Boards Verilog/Active-HDL Edition

By Richard E. Haskell & Darrin M. Hanna

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This book assumes no previous knowledge of digital design. You start at the beginning learning about basic gates, logic equations, Boolean algebra, and Karnaugh maps. In over 75 examples we show you how to design digital circuits using Verilog, simulate them using the Aldec Active-HDL simulator, and synthesize the designs to a Xilinx Spartan3E FPGA on either the BASYS2TM (or BASYSTM) system board that can be purchased from Digilent, Inc (www.digilentinc.com) for $59 or the Nexys-2 board that costs $99. More recently, Digilent offers the Nexys-3 board with a Spartan-6 FPGA that costs $119. A free student edition of the Aldec Active-HDL simulator is available from Aldec, Inc. (www.aldec.com). To synthesize your designs to a Spartan3E FPGA you will need to download the free ISE WebPACK from Xilinx, Inc. (www.xilinx.com). The Xilinx synthesis tools are called from within the Aldec Active-HDL integrated GUI. We will use the Adept 2.1 utility to download your synthesized design to the Spartan3E or Spartan6 FPGA. Adept 2.1 can be downloaded free from Digilent, Inc. (www.digilentinc.com). You should use Adept 2.1 to download your bit files to either the BASYS2, Nexys-2, or Nexys-3 boards. All references to the BASYS board in this book apply to the newer BASYS2 board. The only difference is that if you are using the BASYS board, you must use the user constraints file (.ucf) for the BASYS board (basys.ucf), while if you are using the BAYSY2 board, you must use the user constraints file (.ucf) for the BASYS2 board (basys2board.ucf). Both of these user constraints (.ucf) files can be downloaded from http://www.lbebooks.com/downloads.htm.
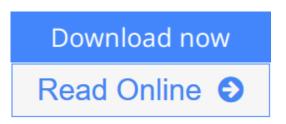
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